

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Gilbert Wolrich et al.                      Art Unit: 2183  
Serial No.: 09/760,509                                      Examiner: Aimee J. Li  
Filed : January 12, 2001  
Assignee : Intel Corporation  
Title : METHOD AND APPARATUS FOR PROVIDING LARGE REGISTER  
ADDRESS SPACE WHILE MAXIMIZING CYCLETIME PERFORMANCE  
FOR A MULTI-THREADED REGISTER FILE SET

**MAIL STOP AMENDMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicants call attention to the attached Information Disclosure Statement and documents listed on form PTO-1449.

The documents are in the English language; hence no concise explanation is necessary per Rule 98(a)(3).

Consideration of the foregoing and enclosures plus the return of a copy of the enclosed form PTO-1449 with the Examiner's initials in the left column per MPEP 609 are earnestly solicited along with an early action on the merits.

Furthermore, Applicants respectfully request consideration of the four Information Disclosure Statements filed in the U.S. Patent and Trademark Office on January 14, 2005 for the instant application. A copy of the four submissions is enclosed (9 pages total).

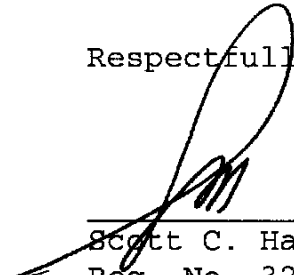
Applicant : Gilbert Wolrich et al.  
Serial No.: 09/760,509  
Filed : January 12, 2001  
Page 2 of 2

Attorney's Docket No.: 10559-317001  
P9678

Kindly accept this Information Disclosure Statement under Rule 97(c)(2). Please apply the rule 17(p) certification fee in the amount of \$180 to deposit account 06-1050.

Respectfully submitted,

Date: February 22, 2007



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10711242.doc

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-317001	Application No. 09/760,509
<b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary)  (37 CFR §1.98(b))		Applicant Gilbert Wolrich et al.	
		Filing Date January 12, 2001	Group Art Unit 2183

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	2002/0038403	03/2002	Wolrich et al.			
	AB	3,577,189	05/1971	Cocke et al.			
	AC	3,881,173	04/1975	Larsen et al.			
	AD	4,454,595	06/1984	Cage			
	AE	4,471,426	09/1984	McDonough			
	AF	4,477,872	10/1984	Losq et al.			
	AG	4,569,016	02/1986	Hao et al.			
	AH	4,742,451	05/1988	Bruckert et al.			
	AI	4,755,966	07/1988	Lee et al.			
	AJ	4,808,988	02/1989	Burke et al.			
	AK	4,816,913	03/1989	Harney et al.			
	AL	4,847,755	07/1989	Morrison et al.			
	AM	4,868,735	09/1989	Moller et al.			
	AN	5,045,995	09/1991	Levinthal et al.			
	AO	5,056,015	10/1991	Baldwin et al.			
	AP	5,165,025	11/1992	Lass			
	AQ	5,170,484	12/1992	Grondalski			
	AR	5,187,800	02/1993	Sutherland			
	AS	5,189,636	02/1993	Patti et al.			
	AT	5,202,972	04/1993	Gusefski et al.			
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	AZ	5,463,746	10/1995	Brodnax et al.			
	BA	5,541,920	07/1996	Angle et al.			

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

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	BB	5,544,337	08/1996	Beard et al.			
	BC	5,572,690	11/1996	Molnar et al.			
	BD	5,600,848	02/1997	Sproull et al.			
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	CA	5,928,358	07/1999	Takayama et al.			
	CB	5,937,177	08/1999	Molnar et al.			

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	CC	5,943,491	08/1999	Sutherland et al.			
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	CK	6,101,599	08/2000	Wright et al.			
	CL	6,115,777	09/2000	Zahir et al.			
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	CN	6,141,348	10/2000	Muntz			
	CO	6,145,123	11/2000	Torrey et al.			
	CP	6,157,988	12/2000	Dowling			
	CQ	6,195,739	02/2001	Wright et al.			
	CR	6,205,468	03/2001	Diepstraten et al.			
	CS	6,223,208	04/2001	Kiefer et al.			
	CT	6,223,277	04/2001	Karguth			
	CU	6,230,119	05/2001	Mitchell			
	CV	6,230,230	05/2001	Joy et al.			
	CW	6,230,261	05/2001	Henry et al.			
	CX	6,259,699	07/2001	Opalka et al.			
	CY	6,275,508	08/2001	Aggarwal et al.			
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	DB	6,338,133	01/2002	Schroter			
	DC	6,378,124	04/2002	Bates et al.			

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	DE	6,385,720	05/2002	Tanaka et al.			
	DF	6,401,155	06/2002	Saville et al.			
	DG	6,408,325	06/2002	Shaylor			
	DH	6,446,190	09/2002	Barry et al.			
	DI	6,496,847	12/2002	Bugnion et al.			
	DJ	6,505,229	01/2003	Turner et al.			
	DK	6,523,108	02/2003	James et al.			
	DL	6,543,049	04/2003	Bates et al.			
	DM	6,560,629	05/2003	Harris			
	DN	6,560,671	05/2003	Samra et al.			
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	DR	6,862,676	03/2005	Knapp et al.			
	DS	6,976,095	12/2005	Wolrich et al.			
	DT	6,983,350	01/2006	Adiletta et al.			
	DU	7,020,871	03/2006	Bernstein et al.			

### Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	DV	0 130 381	01/1985	Europe				
	DW	0 463 855	01/1992	Europe				
	DX	0 476 628	03/1992	Europe				
	DY	0 696 772	02/1996	Europe				
	DZ	WO 01/18646	03/2001	WIPO				
	EA	WO03/019399	03/2003	WIPO				

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							Yes	No
	EB	WO03/085517	10/2003	WIPO				

### Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	EC	"HART, Field Communications Protocol, Application Guide", Hart Communication Foundation, pp. 1-74, (1999).
	ED	Bowden, Romilly, "What is HART?" Romilly's HART® and Fieldbus Web Site, 3 pages, (1997). <URL: <a href="http://www.romilly.co.uk/whathart.htm">http://www.romilly.co.uk/whathart.htm</a> >
	EE	Cheng, et al., "The Compiler for Supporting Multithreading in Cyclic Register Windows", <i>IEEE</i> , pp. 57-62, (1996).
	EF	Hennessy et al., <i>Computer Organization and Design: The Hardware/Software Interface</i> , Morgan Kaufman Publishers, pp. 116-119, 181-182, 225-227, 447-449, 466-470, 476-482, 510-519, 712, (1998).
	EG	Heuring et al., <i>Computer Systems Design and Architecture</i> , Reading, MA, Addison Wesley Longman, Inc., pp. 38-40, 143-171, and 285-288, (1997).
	EH	Hidaka, Y., et al., "Multiple Threads in Cyclic Register Windows", <i>Computer Architecture News</i> , ACM, New York, NY, USA, 21(2):131-142, May 1993.
	EI	Hirata, H., et al., "An Elementary Processor Architecture with Simultaneous Instruction Issuing from Multiple Threads", <i>Proc. 19th Annual International Symposium on Computer Architecture, ACM &amp; IEEE-CS</i> , 20(2):136-145, May 1992.
	EJ	Intel, "1A-64 Application Developer's Architecture Guide," Rev.1.0, pp. 2-2, 2-3, 3-1, 7-165, C-4, and C-23, May 1999.
	EK	Koch, G., et al., "Breakpoints and Breakpoint Detection in Source Level Emulation", <i>Proc. 19th International Symposium on System Synthesis (ISSS '96)</i> , <i>IEEE</i> , pp. 26-31 (1996).
	EL	Moors, et al., "Cascading Content-Addressable Memories", <i>IEEE Micro</i> , 12(3):56-66 (1992).
	EM	Okamoto, K., et al., "Multithread Execution Mechanisms on RICA-1 for Massively Parallel Computation", <i>IEEE - Proc. Of PACT '96</i> , pp. 116-121 (1996).
	EN	Patterson, et al., <i>Computer Architecture A Quantitative Approach</i> , 2nd Ed., Morgan Kaufmann Publishers, Inc., pp. 447-449, (1996).
	EO	Paver, et al., "Register Locking in an Asynchronous Microprocessor", <i>IEEE</i> , pp. 351-355, (1992).
	EP	Philips ED - Philips Components: "8051 Based 8 Bit Microcontrollers, Data Handbook Integrated Circuits, Book IC20", 8051 Based 8 Bit Microcontrollers, Eindhoven, Philips, NL, pp. 5-19 (1991).
	EQ	Probst et al., "Programming, Compiling and Executing Partially-Ordered Instruction Streams on Scalable Shared-Memory Multiprocessors", <i>Proceedings of the 27th Annual Hawaiian International Conference on System Sciences, IEEE</i> , pp. 584-593, (1994).
	ER	Quammen, D., et al., "Flexible Register Management for Sequential Programs", <i>IEEE Proc. of the Annual International Symposium on Computer Architecture</i> , Toronto, May 27-30, 1991, vol. SYMP. 18, pp. 320-329.
	ES	Ramsey, N., "Correctness of Trap-Based Breakpoint Implementations", <i>Proc. of the 21st ACM Symposium on the Principles of Programming Languages</i> , pp. 15-24 (1994).

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		Filing Date January 12, 2001	Group Art Unit 2183

<b>Other Documents (include Author, Title, Date, and Place of Publication)</b>		
Examiner Initial	Desig. ID	Document
	ET	Steven, G.B., et al., "ALU design and processor branch architecture", <i>Microprocessing and Microprogramming</i> , 36(5):259-278, October 1993.
	EU	Young, H.C., "Code Scheduling Methods for Some Architectural Features in Pipe", <i>Microprocessing and Microprogramming</i> , Elsevier Science Publishers, Amsterdam, NL, 22(1):39-63, January 1988.
	EV	Young, H.C., "On Instruction and Data Prefetch Mechanisms", <i>International Symposium on VLSI Technology, Systems and Applications, Proc. of Technical Papers</i> , pp. 239-246, (1995).

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# ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

## Title of Invention

METHOD AND APPARATUS FOR PROVIDING LARGE  
REGISTER ADDRESS SPACE WHILE MAXIMIZING CYCLETIME  
PERFORMANCE FOR A MULTI-THREADED REGISTER FILE SET

Application Number : 09/760509



Confirmation Number: 2157

First Named Applicant: Gilbert Wolrich

Attorney Docket Number: 10559-317001

Art Unit: 2183

Examiner: Barry J. OBrien

Search string: ( 6223238 or 6223279 or 6247025 or 6256713 or 6272616 or 6275505 or 6279113  
or 6289011 or 6298370 or 6307789 or 6324624 or 6345334 or 6347344 or 6351808  
or 6356962 or 6373848 or 6360262 or 6389449 or 6393483 or 6415338 or 6426940  
or 6427196 or 6430626 or 6434145 or 6463072 or 6532509 or 6552826 or 6560667  
or 6577542 or 6584522 or 6587906 or 6606704 or 6625654 or 6629237 or 6631430  
or 6631462 or 6661794 or 6667920 or 6668317 or 6681300 or 6694380 or 4023023  
or 5113516 or 5363448 or 5436626 or 5600812 or 5652583 or 5717760 or 4992934  
or 5450603 ).pn

## US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
	1	6223238	2001-04-24	Meyer et al.			
	2	6223279	2001-04-24	Nishimura et al.			
	3	6247025	2001-06-12	Bacon			
	4	6256713	2001-07-03	Audityan et al.			
	5	6272616	2001-08-07	Fernando et al.			
	6	6275505	2001-08-14	O Loughlin et al.			
	7	6279113	2001-08-21	Vaidya			
	8	6289011	2001-09-11	Seo et al.			
	9	6298370	2001-10-02	Tang et al.			
	10	6307789	2001-10-23	Wolrich et al.			
	11	6324624	2001-11-27	Wolrich et al.			
	12	6345334	2002-02-05	Nakagawa et al.			
	13	6347344	2002-02-12	Baker et al.			
	14	6351808	2002-02-26	Joy et al.			
	15	6356962	2002-03-12	Kasper et al.			
	16	6373848	2002-04-16	Allison et al.			
	17	6360262	2002-03-19	Guenthner et al.			

18	6389449	2002-05-14	Nemirovsky et al.			
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20	6415338	2002-07-02	Habot			
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25	6463072	2002-10-08	Wolrich et al.			
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**Signature**

Examiner Name	Date

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init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
	1	5937187	1999-08-10	Kosche et al.			
	2	5938736	1999-08-17	Muller et al.			
	3	5940612	1999-08-17	Brady et al.			
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	17	6014729	2000-01-11	Lannan et al.			

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**Signature**

Examiner Name	Date

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Stylesheet Version v18.0

## Title of Invention

METHOD AND APPARATUS FOR PROVIDING LARGE  
REGISTER ADDRESS SPACE WHILE MAXIMIZING CYCLETIME  
PERFORMANCE FOR A MULTI-THREADED REGISTER FILE SET

Application Number : 09/760509



Confirmation Number: 2157

First Named Applicant: Gilbert Wolrich

Attorney Docket Number: 10559-317001

Art Unit: 2183

Examiner: Barry J. OBrien

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or 5623489 or 5627829 or 5630130 or 5644623 or 5649157 or 5659722 or 5680641  
or 5689566 or 5692167 or 5699537 or 5717898 or 5721870 or 5742587 or 5742782  
or 5742822 or 5745913 or 5751987 or 5761507 or 5761522 or 5781774 or 5784649  
or 5784712 or 5796413 or 5797043 or 5809235 or 5809530 or 5812839 or 5812868  
or 5828746 or 5828863 or 5832215 or 5835755 or 5854922 or 5860158 or 5886992  
or 5887134 or 5890208 or 5892979 or 5905876 or 5905889 or 5915123 or 5933627  
or 5659687 ).pn

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Note: Applicant is not required to submit a paper copy of cited US Patent Documents

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**Signature**

Examiner Name	Date

# ELECTRONIC INFORMATION DISCLOSURE STATEMENT

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Examiner Name	Date